International Journal of Advances in Engineering and Management (IJAEM)
Volume 5, Issue 9 Sep 2023, pp: 276-281 www.ijaem.net ISSN: 2395-5252

Stability Analysis of a Novel Proposed Low Power 14t SRAM Cell

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Date of Submission: 15-09-2023 Date of Acceptance: 25-09-2023

ABSTRACT: In modern high performance integrated circuits, maximum of the total active mode energy is consumed due to leakage current. SRAM array is main source of leakage current since majority of transistor are utilized for on chip memory in today high performance microprocessor and system on chip. Therefore low leakage SRAM is required. The designed 14T SRAM cell provides less power consumption and delay. The simulation results such as power dissipation and delay of the proposed SRAM cell have been calculated and contrasted. The proposed configuration gives diminishment in power dissipation. For design and simulation purpose, Tanner EDA Tool V.14.1 at 45nm CMOS has been used.

KEYWORDS: SRAM, 14T, Tanner EDA Tool, CMOS.

I. INTRODUCTION

Power dissipation instead of performance is mainly concerned in the chip design nowadays. Since a major Part of chip power is occupied by SRAM. Low power SRAM is urgently needed. The portable microprocessor controlled devices, embedded memory, which represented a larger portion of the system on chip. These portable systems need ultra low power consumption, it can be minimized and also recently the demand for low power battery operated device is grown and where needed to low supply voltage. Low power SRAM are required to extend system operation time under limited energy resources. This method reduces both switching power and leakage power for CMOS VLSI and designing 14T sub-threshold SRAM cell. This method removes the half-select issue in 6T, 8T, 10T and 12T SRAM cell and provides faster read and write operation. Since the proposed cell is free from half-select disturb, SRAM cell is better hold noise margin and write performance compared to the 12T SRAM cell. The half selected cell problem in write operation is eliminated, which makes SRAM cell robust in sub threshold region.

SRAM CELL: SCHEMATIC AND WORKING

Fig 1 represents the memory cell of SRAM for an individual bit. The latches which are static are deployed in cell of SRAM. The cell is formulated from a flip flop that is consisted of inverters which are coupled as cross. Fig1 Schema for cell of SRAM. The transistors of access which are 2 in number are deployed to evaluate the information retained in cell. The line for control that is WL, word line turns the transistors OFF or ON. In general, the WL is linked to outcome of circuitry of decoder of row. As the WL is equal to V_{dd}, BL is linked to cell of SRAM and it's complementary, which allows both write & read operations. The function of read & write is executed by transistors of access.

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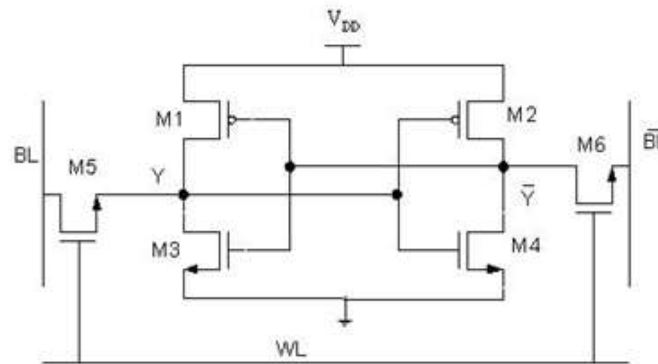

Fig 1:- Schematic SRAM Cell

Static Random-Access Memory (SRAM) could be a style of semiconductor memory that uses bi-stable latching electronic equipment to store every bit. This term static differentiates it from Dynamic RAM (DRAM) that should be sporadically invigorated. SRAM exhibits knowledge remembrance; however it is still volatile within the typical sense that knowledge is eventually lost once the memory isn't steam-powered. For increasing the battery standby time it is coming up with a replacement style of SRAM cell that consumes less power than the prevailing SRAMs. The key objective behind this paper is to cut back the facility consumption of Random Access Memory.

II. EXISTING SRAM CELLS

This section revolves round the performance comparison of SRAM cells consisting of various varieties of transistors wont to store single bit. From last four decades, we have a tendency to square measure cutting down the CMOS devices to realize the higher performance in terms of speed, power consumption, noise margins, delay etc. SRAM based mostly cache recollections square measure ordinarily used because of their higher speed. However because of device scaling there is a tendency to face style challenges for micro millimeter SRAM style. Owing to low threshold voltage and extremist skinny gate compound, the outpouring energy consumption is obtaining increased. During this section performance analysis of 6T, 8T and 9T has been carried under power consumption and delay[2].

6T SRAM Cell

There is a unit many topologies for SRAM in past decades 6T SRAM got its attention for the tolerance capability for noise over another SRAM cell style. The 6T SRAM cell vogue consists of two access transistors and a couple of cross coupled CMOS inverters. Bit lines unit the input/output ports of the cell with high physical phenomenon loading. The operations browse and WRITE unit conducted by these bit lines entirely, can be tend to unit going to see but these are administrated. **Write Operation:** For writing 1/0 we must always give the info to the bit line (BL), with relation to the bit line bar ((BL)̅). Once the word line (WL) is enabled the info is written into several nodes.

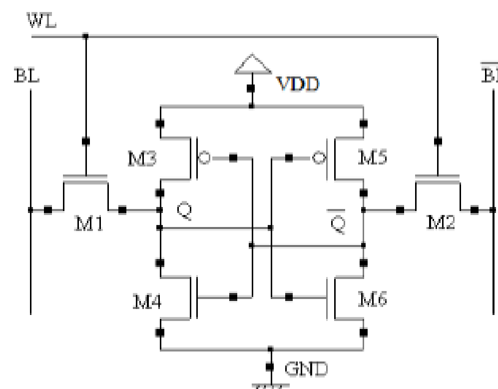

Fig 2 Conventional 6T SRAM

But the conventional 6T SRAM have stability limitations at low supply voltages as shown

in Fig2. Hence we go for 8T SRAM design. It has the advantage of low power at read "1" operation. It does not consume power at read "1" cycle.

8T SRAM Cell

8T cells that are much more robust as compared to the 6T cells due to isolated read port. We show that without modifying the basic bit-cell for the 8T SRAM cell, it is possible to configure the 8T cell for in-memory dot product computations. Note, in sharp contrast to the previous works on in-memory computing with the CMOS technology, we enable current based, analog like dot product computations using robust digital 8T bit-cells.

1) We show that the conventional 8T SRAM cell can be used as a primitive for analog like dot product computations, without modifying the bit-cell circuitry. In addition, we present two different configurations for enabling dot product computation using the 8T cell.

2) Apart for the sizing of the individual transistors consisting of the read port of the 8T cell, the basic bit-cell structure remains unaltered. Thereby, the 8T SRAM array can also be used for usual digital memory read and write operations. As such, the presented 8T cell array can act as a dedicated dot product engine or as an on-demand dot product accelerator.

3) A detailed simulation analysis using 45nm predictive technology models including layout analysis and effect of non-idealities like the existence of line-resistances and variation in transistor threshold voltages has been reported highlighting the various trade-offs presented by each of the two proposed configurations.

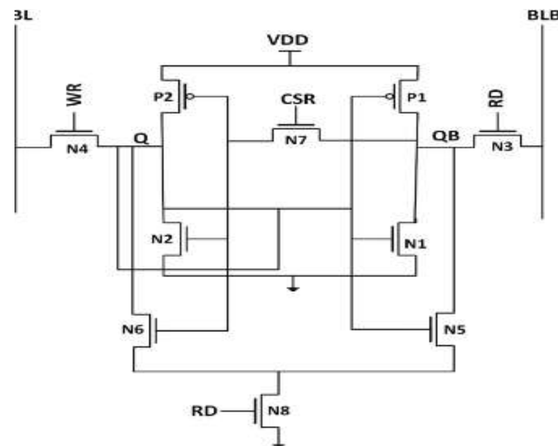

Fig 3 Conventional 8T SRAM

The memory bit cell remains in standby mode when it is not being accessed in read or write operation. During standby mode, the memory bit cell continually consumes little power that is widely known as leakage power. At deep sub-micro-metre nodes leakage power has emerged as a serious matter in embedded cache memory design. The state of different transistors of proposed 8T SRAM cell during idle mode is depicted in Fig 3.

The transistors with crossed sign symbol in Fig 3 displays off state. Since WR and RD signals are in off state, therefore, significant contribution to the leakage power is made by core latch of circuit. The collective effect of wide access transistors, read buffer transistors and read stack transistor in addition to leakage of core latch leads to higher leakage power of proposed 8T circuit in comparison with conventional 6T SRAM cell. As detailed in device sizing guidelines, the transistors in core latch are kept at lesser width. Also, the leakage path of read buffer transistors is blocked by switched off read stack transistor.

10T SRAM Cell

Fig 4 shows the conventional 10T SRAM cells with a high level of read and write stability and capability. A Schmitt-trigger inverter with a double-length pull-up transistor and a regular inverter with a stacking transistor make up the robust cross-coupled construction of the proposed 10T SRAM cell. The read-disturbance is eliminated as a result of this and the read path being set apart from real internal storage nodes. Additionally, it uses a write-assist mechanism and executes its write operation in pseudo differential form using a write bit line and control signal. To estimate the proposed 10T SRAM cell's performance, it is compared with some state-of-the-art SRAM cells using TANNER EDA in 45-nm CMOS predictive technology model at 0.7 V supply voltage under harsh manufacturing process, voltage, and temperature variations cell it indicates

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working nature of the cross coupled inverters the word line is maintained at 0.7v constantly, QA is compliment to bit line (BL) and QB is compliment to bit line bar (BLB) as shown in the Fig.

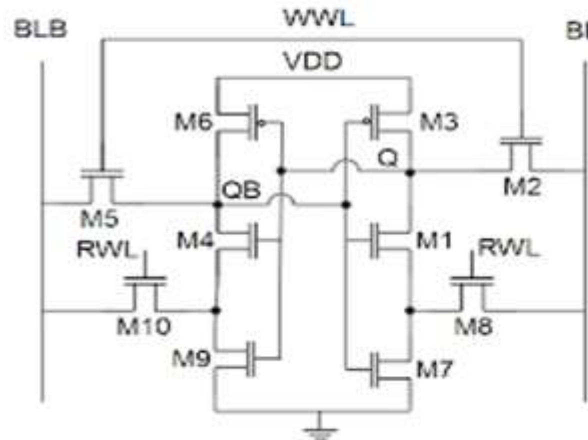

Fig 4 Conventional 10T SRAM

Designing an SRAM array initially, the SRAM Array's design sub-circuits are fundamental circuits that are very important to the design of the SRAM Array. These are the SRAM cell, Write Driver, Sense Amplifier, Pre-charge Circuit, and 3 to 8 Decoder.

There is a problem when read "1" operation is performed, a small leakage current flows known as bit line leakage. To overcome this problem, one more transistor is used in read path. By using another transistor bit line leakage is reduced and this process is called stacking effect. Fig 4 10T SRAM cell to decrease read power, RBL swing is reduced. When read "0" is performed charge sharing is done between RBL and BLB or RBL and BL accordingly whether last data written is "1‟ or "0‟ respectively. RBL is not discharged properly because of charge sharing, and it remains at middle-level of voltage, during next cycle pre-charge circuit uses less power. The bit line is driven from middle-voltage value to full swing voltage. To decrease write operation power write driver is used. The bit line is driven high or low using write driver according to the data value. When read "0‟ is performed the read discharge flow via read path and M9 to BL, so BL is somewhat charged. During next write "1‟ BL is driven to "1‟ from middle-level voltage using write driver. This decrease the power and this can only be done after read "0‟.

12T SRAM Cell

This method implemented to decrease write and read energy consumption in order to maintain high data reliability and write skills on the current 12 T SRAM low power circuit. With the use of advanced 45-nm CMOS materials, all transistors in SRAM cells use smallest channel length (45 nm) and channel width (45 nm) [3]. The transistor has shared the every column of SRAM cells. For physical design, the proposed static random access cell has been implemented and described as a standard cell and are treated in analogous manner to the sleep transistors utilized while routing and planning. The proposed method can handle an up to 4 bit that consists of a block. Such four bits are interpreted by mask transistors, gate transistors and four pair of intertwined cross coupled inverters, read buffer and writer entry transistors. Based on the stacked nMOS configuration theory, the read buffer is used [1] [2]. The leakage voltage has been avoided by this configuration. It contains of a line to pick the signal you need, called as BPS [Block Pick Signal]. The typical 12T cell process is carried on as follows. BPS is set to 0V to enforce write operation. And therefore the word line is permitted. Likewise, BPS is set at 1V for a read operation, as well as the word line is stopped. Therefore the line of terms serves as an ON OFF turn [4]. Fig 5 shows the schematic representation of the proposed methodology for the design of 12T static random access memory.

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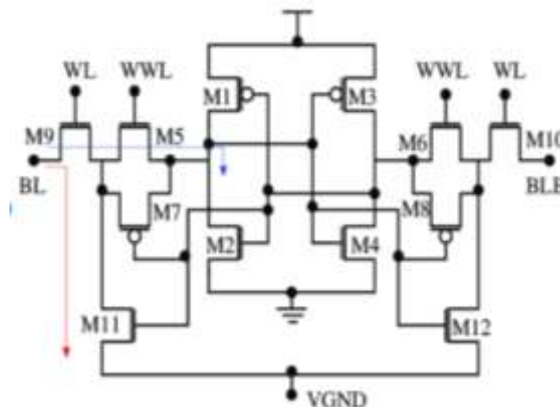

Fig 5 Conventional 12T SRAM

For LBL to discharge, a supply voltage VDD is carried out. This will shut the read buffers off, in effect. In the meantime, the full VDD supply voltage has preloaded to RBLs and the word lines are retained at 0V.During the read process, the block mask transistors are enforced to persist in the OFF place. To hold the transistor in ON stage, the word line is restricted for the transfer accesses. As a consequence, through the pass gate transistor the data stored in a single cell is distributed to the RBL from LBL. When the data is stored, it discharges the RBLs. These RBLs are located on the blocks of the given column and row. After the read process ends, word lines are connected at zero voltage to switch OFF the transistors pass-gate. The best way to minimize energy consumption through the use of 12T SRAM is to do so. It minimizes energy consumption as a result of standby, read wait, writing delays, etc. Experimentally demonstrated by implementing the parallel cross coupling logic in 12T SRAM, which is the best way to save energy use and operating delays. The size of memory cell is also minimized with the lower processing nodes. The current memory cell leakage factor will be increased thereby. The intersection of leakage, gate leakage and multi threshold leakage current are various additives which triggers the 12T static random access memory cell leakage. However in lower-technologies, multi threshold leakage current is predominant. When the leakage current is off, the voltage of transistor gate is less than the voltage at its highest and contains mostly of a diffusion stream; the transistor gate voltage is the lowest.

14T SRAM Cell

In this present work a low power 14T SRAM cell is proposed. A charge recycling technique is used to minimize the leakage currents and static power dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swig voltages, resulting in reduction of dynamic power dissipation during switching activity. The different performance parameters have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells.

The proposed gate oxide overlap heterojunction tunnel transistor is not only works best for basic SRAM cells such as 6T, 7T, 8T, 9T and 10T circuits, but it is doing well for higher versions of SRAM circuits. Here, we considered radiation hardened 14T SRAM cell with high speed and power optimized which is used for space applications and the traditional devices are replaced by the proposed devices. The radiation hardened 14T SRAM cell is shown in fig 6.

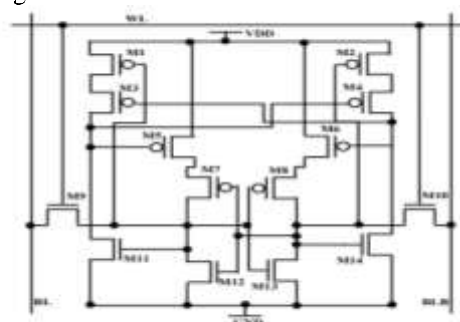

Fig 6 Conventional 14T SRAM

Table 1 shows the comparison of 6T, 8T, 10T, 12T and 14T performance. With this it is concluded that 14T has the low power dissipation and less delay when compared to 6T, 8T, 10T and 12T.

S.No	Parameter	6T SRAM	8T SRAM	10T SRAM	12T SRAM	14T SRAM
1	Technology	45nm	45nm	45nm	45nm	45nm
2	Supply Voltage	700mV	700mV	700mV	700mV	700mV
3	Power Dissipation	19.1nW	24.4nW	12.1nW	1.98µW	0.80µW
4	Write Delay	110ps	81.7ps	50ps	24.22ps	18.12ps

Table 1. Comparison of 6T, 8T, 10T, 12T and 14T performance

III. CONCLUSION

The technology changes day by day. Power dissipation and stability are major issue of any high speed device. The proposed SRAM cell is the solution of this problem, which used 14T SRAM cell and gives less power dissipation and delay. The new design was compared to existing design using simulation in the 45nm CMOS technology. Simulation has been done with different transistors of SRAM Cell. In this technique the 14T SRAM cell gives less power dissipation and delay compared to 6T, 8T, 10T and 12T SRAM cell.

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